200MHz to 3GHz High Linearity Y-Mixer

Preliminary Technical Data

ADL5350

FEATURES

Broadband RF, IF and LO Ports
Low Conversion Loss
Noise figure : 6dB
High Input IP3: 26dBm
High Input P_{1dB}: 17dBm
Low LO drive level
Single-Ended Design: No Need for Baluns
Single-supply operation: 3V @ 16mA
Miniature 8-Lead 3 x 2mm CSP Package
RoHS Compliant

APPLICATIONS

Cellular base station
Point-to-Point Radio links
RF Instrumentation

FUNCTIONAL BLOCK DIAGRAM

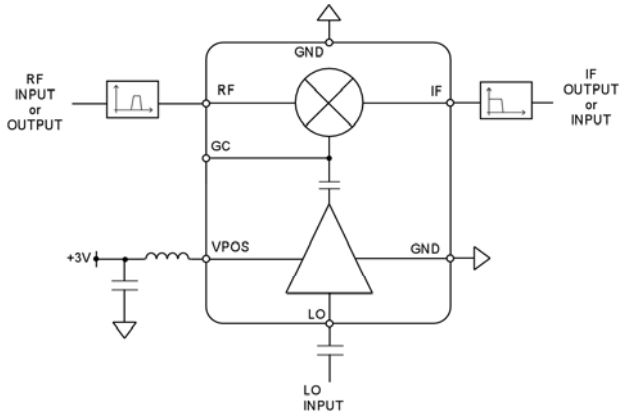

Figure 1.

GENERAL DESCRIPTION

The ADL5350 is a high linearity up and down converting mixer capable of operating over a broad input frequency range. It is well suited for demanding cellular base-station mixer designs that require high sensitivity and good blocker immunity. Based on a GaAs pHEMT single-ended mixer architecture, the ADL5350 provides excellent input linearity and low noise figure without the need for high power level LO-drive.

In 850/900MHz receive applications the ADL5350 provides a typical conversion loss of only 6dB. The integrated LO amplifier allows a low LO drive level, typically only 4dBm for most applications. The input IP3 is typically greater than 25dBm, with an input compression point of 17dBm. The high input linearity of the ADL5350 makes the device an excellent mixer for communications systems that require high blocker immunity, such as GSM 850/900 and 800MHz CDMA2000. At 2GHz, a slightly greater supply current is required to obtain similar performance.

For low frequency applications the ADL5350 provides access to the gate contact of the output mixing device. This allows an external LO coupling capacitor to be applied between the VPOS and GC pins, helping to improve the LO drive to the switching device. Using a single 100pF capacitor allows for high performance at the lower LO frequencies.

The single-ended broadband RF/IF port allows the device to be customized for a desired band of operation using simple external filter networks. The LO to RF isolation is determined based on the LO rejection of the RF port filter network. Greater isolation may be achieved using higher order filter networks as described in the applications section of the datasheet.

The ADL5350 is fabricated on a GaAs pHEMT high performance IC process. The ADL5350 is available in a 3x2mm 8-lead CSP package. It operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. PrB

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SPECIFICATIONS

800MHz Receive Performance

V_S = 3 V, T_A = 25°C, LO power = 4 dBm, re: 50 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency Range		800	850	900	MHz
LO Frequency Range	High Side LO	730	780	830	MHz
IF Frequency Range			70		MHz
Conversion Loss	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz		6		dB
SSB Noise Figure	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz		6		dB
Input Third-Order Intercept	f_{RF1} = 819MHz, f_{RF2} = 821 MHz, f_{LO} = 750 MHz f_{IF} = 70 MHz, each RF tone 0 dBm		26		dBm
Input Second-Order Intercept	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz		33		dBm
Input 1 dB Compression Point	f_{RF} = 820 MHz, f_{LO} = 750 MHz, f_{IF} = 70 MHz		17		dBm
LO to IF Leakage	LO Power = 4 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz		-21		dBc
LO to RF Leakage	LO Power = 4 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz		-15		dBc
RF to IF Leakage	RF Power = 0 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz		-22		dBc
IF/2 Spurious	RF Power = 0 dBm, f_{RF} = 820 MHz, f_{LO} = 750 MHz		-42		dBc
Supply Voltage		2.7	3	5.5	V
Supply Current	LO Power = 4 dBm		16		mA

1950MHz Receive Performance

V_S = 3 V, T_A = 25°C, LO power = 4 dBm, re: 50 Ω, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
RF Frequency Range		1800	1950	2000	MHz
LO Frequency Range	High Side LO	1610	1760	1810	MHz
IF Frequency Range			190		MHz
Conversion Loss	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz		7.5		dB
SSB Noise Figure	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz		7.5		dB
Input Third-Order Intercept	f_{RF1} = 1949 MHz, f_{RF2} = 1951 MHz, f_{LO} = 1760 MHz f_{IF} = 190 MHz, each RF tone 0 dBm		25		dBm
Input Second-Order Intercept	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz		31		dBm
Input 1 dB Compression Point	f_{RF} = 1950 MHz, f_{LO} = 1760 MHz, f_{IF} =190 MHz		16		dBm
LO to IF Leakage	LO Power = 4 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz		-14		dBc
LO to RF Leakage	LO Power = 4 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz		-11		dBc
RF to IF Leakage	RF Power = 0 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz		-10		dBc
IF/2 Spurious	RF Power = 0 dBm, f_{RF} = 1950 MHz, f_{LO} = 1760 MHz		-35		dBc
Supply Voltage		2.7	3	5.5	V
Supply Current	LO Power = 4 dBm		35		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	TBD V
RF Input Level	TBD dBm
LO Input Level	TBD dBm
Internal Power Dissipation	TBD mW
θ_{JA}	TBD °C/W
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

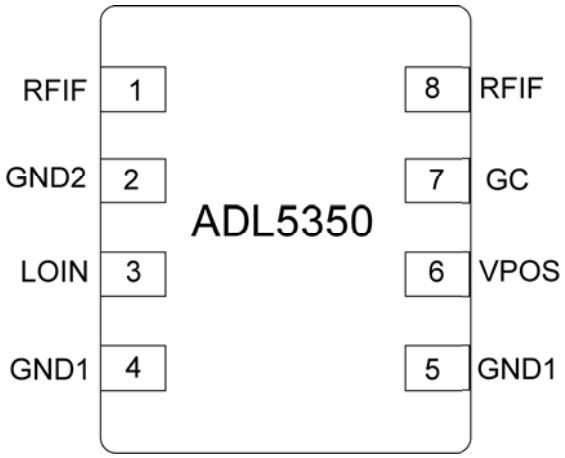

Figure 2. 16-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 8	RFIF	RF and IF input/output ports. These nodes are internally tied together. RF and IF port separation is achieved using external tuning networks.
2	GND2	Device Common (DC Ground) for RFIF switching circuitry.
3	LOIN	LO Input, ac-coupled.
4, 5	GND1	Device Common (DC Ground) for LO buffer circuitry.
6	VPOS	Positive supply voltage for the drain of the LO buffer. A series RF choke is needed on the supply line to provide proper ac-loading of the LO buffer amplifier.
7	GC	Gate Contact of mixing device. Typically not connected for high frequency mixing. Connecting capactor between GC and VPOS permits low frequency applications.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3 V, T_A = 25°C, RF power = 0 dBm, LO power =4dBm, Z_O = 50 Ω, unless otherwise noted.

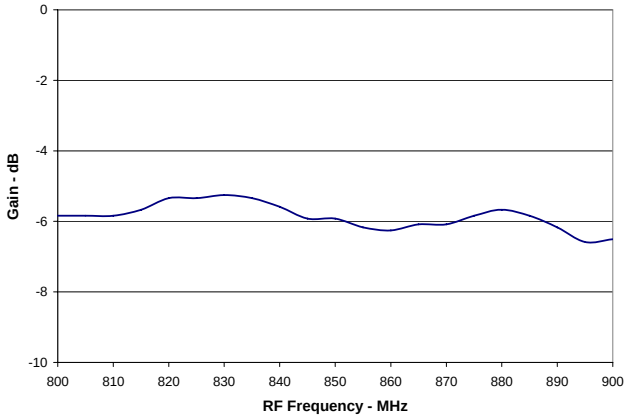

Figure 3. Conversion Loss vs. RF Frequency for 70MHz IF

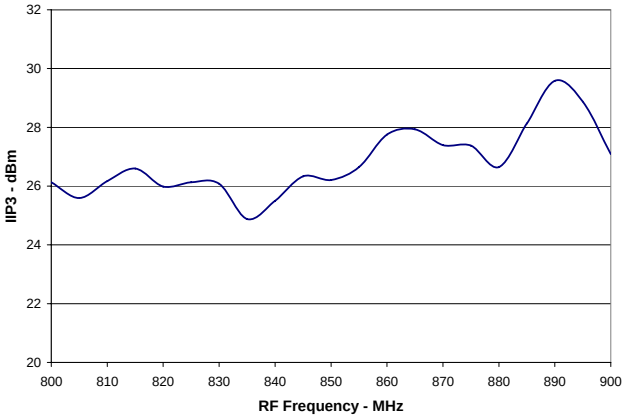

Figure 6. IIP3 vs. RF Frequency for 70MHz IF

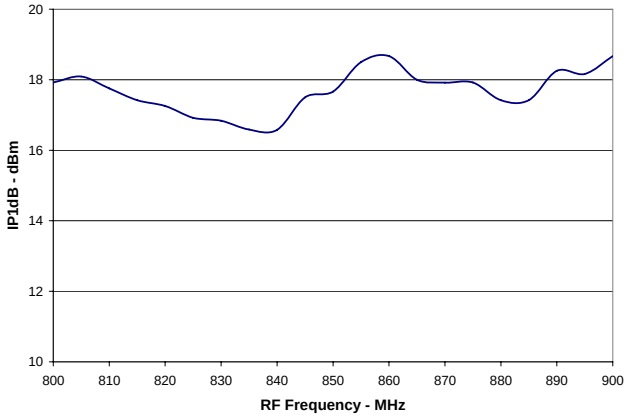

Figure 4. Input 1dB Compression Point vs. RF Frequency for 70MHz IF

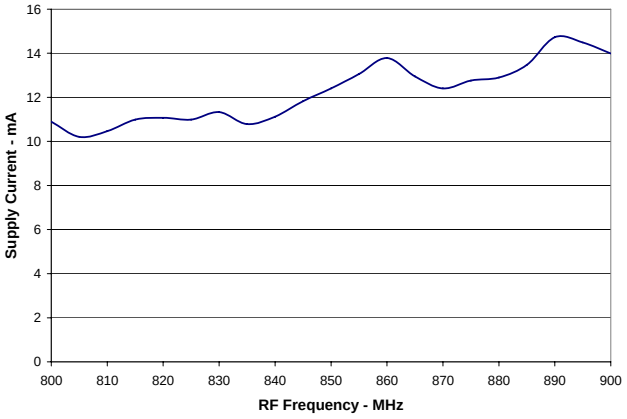

Figure 7. Supply Current vs. RF Frequency for 70MHz IF

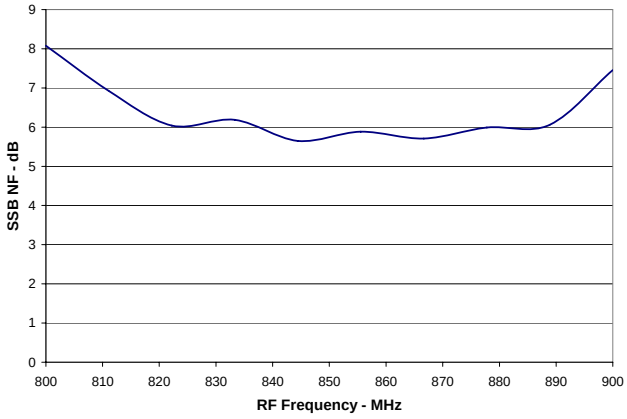

Figure 5. Noise Figure vs. RF Frequency for 70MHz IF

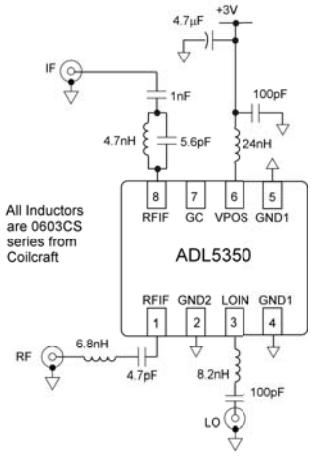

Figure 7. Test Circuit for Figures 3-7, 4dBm LO drive, 3V Supply

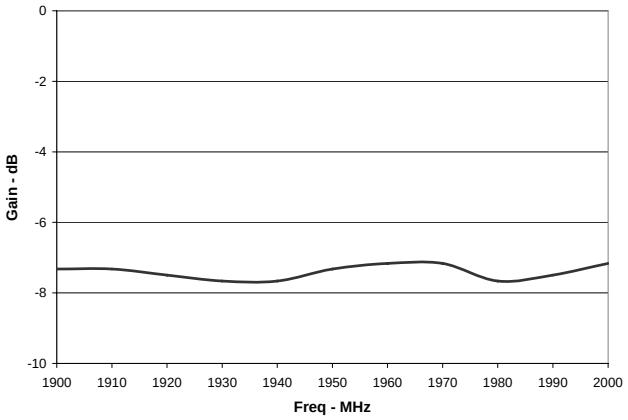

Figure8. Conversion Loss vs. RF Frequency for 190MHz IF

Figure 11. IIP3 vs. RF Frequency for 190MHz IF

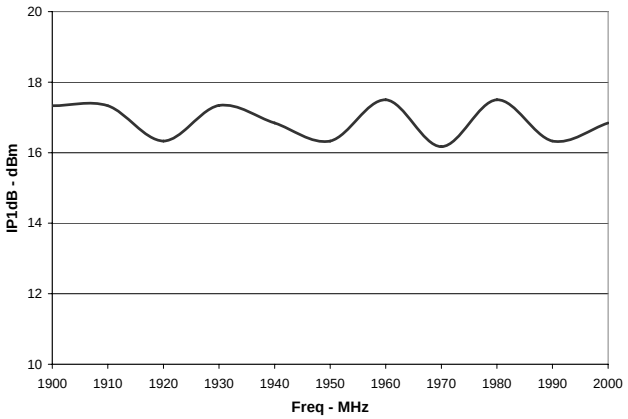

Figure 9. Input 1dB Compression Point vs. RF Frequency for 190MHz IF

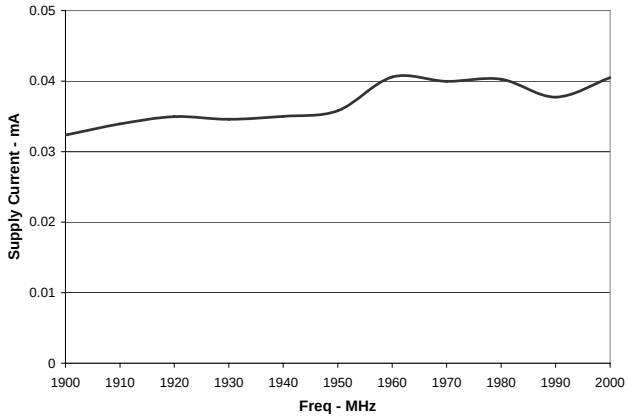

Figure 12. Supply Current vs. RF Frequency for 190MHz IF

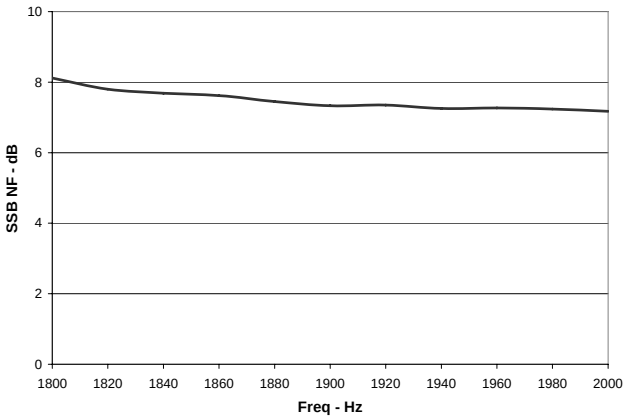

Figure 10. Noise Figure vs. RF Frequency for 190MHz IF

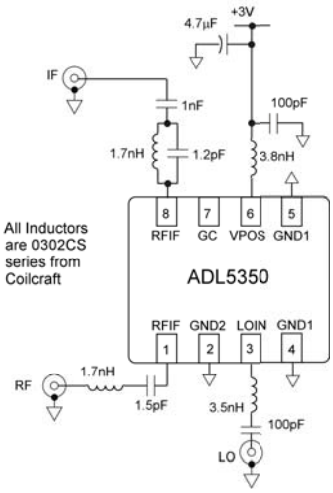

Figure13. Test Circuit for Figures 9-12, 4dBm LO drive, 3V Supply

CIRCUIT DESCRIPTION

The ADL5350 is a GaAs MESFET single-ended passive mixer with an integrated LO buffer amplifier. The device relies on the varying drain to source channel conductance of a FET junction to modulate an RF signal. A simplified schematic is provided below in Figure 14.

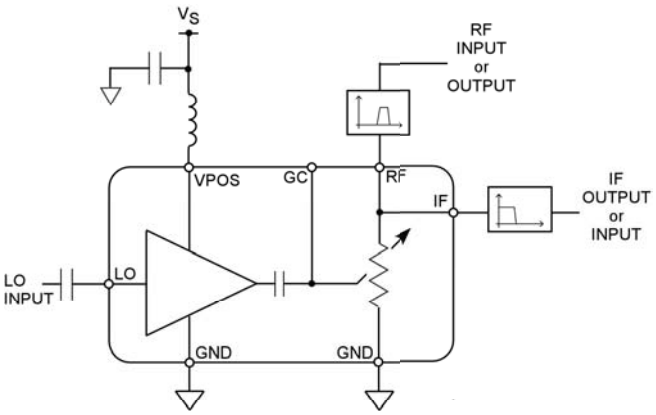

Figure 14. Simplified Schematic

The LO signal is applied to the gate contact of a FET-based buffer amplifier. The buffer amplifier provides sufficient gain of the LO signal to drive the resistive switch. Additionally, feedback circuitry (not shown) provides the necessary bias to the FET buffer amplifier and RF/IF ports to achieve optimum modulation efficiency for common cellular frequencies. The GC node is the 'gate-contact' of the RF/IF port resistive switch (really just a second FET junction). The GC node enables external control of the bias level of the switching FET, allowing the user to override the internal bias generation circuitry and allow further optimization of the dynamic performance of the mixer at frequencies outside of the 800 to 2000MHz band.

Mixing of the RF and LO signals is achieved by switching the channel conductance from the RF/IF port to ground at the rate of the LO. The RF signal is passed through an external band-pass network to help reject image bands and reduce the broadband noise presented to the mixer. The band-limited RF signal is presented to the time varying load of the RF/IF port causing the envelope of the RF signal to be amplitude modulated at the rate of the LO. A filter network applied to the IF port is necessary to reject the RF signal and pass the wanted mixing product. In a down-conversion application the IF filter network is designed to pass the difference frequency and present an open circuit to the incident RF frequency. Similarly for an up-conversion application the filter is designed to pass the sum frequency and reject the incident RF. As a result the frequency response of the mixer is determined by the response characteristics of the external RF/IF filter networks.

IMPLEMENTATION PROCEDURE

The ADL5350 is a simple single-ended mixer that relies on off-chip circuitry to achieve good RF dynamic performance. The following steps should be followed to achieve optimum performance. Please refer to Figure 15 for component designations.

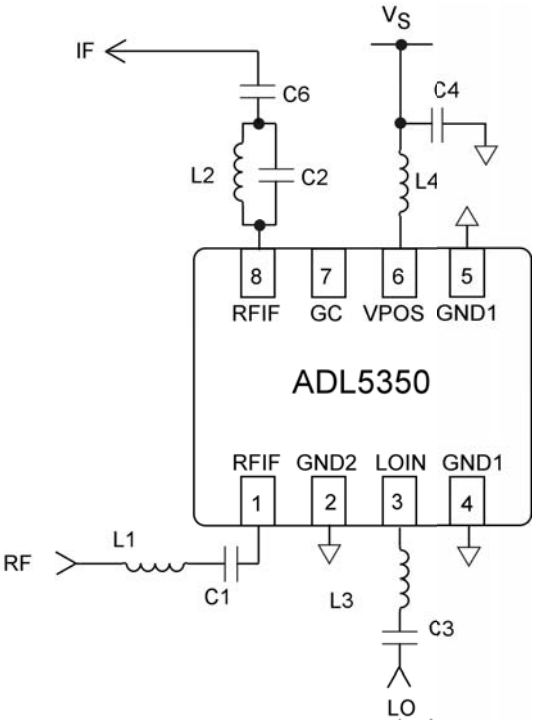

Figure 15. Reference Schematic

1) Tune LO buffer supply inductor for lowest supply current.

In order to start this procedure it is necessary to provide an initial guess. The following table can be used as a starting point. It is not necessary to terminate or populate the RF and IF port networks to complete this first step, the RFIF pins can be left open while tuning the LO buffer networks.

Table 5. Recommended LO Bias Inductor

Desired LO frequency	**Recommended LO bias inductor (L4)**
750MHz	24nH
1000MHz	18nH
1750MHz	3.8nH
2000MHz	2.7nH

In order to test the supply current consumption, simply power up the device and apply the desired LO signal. Attempt to increase and decrease the LO frequency. If the current consumption increases as the LO frequency is decreased, try increasing the value of L4. If the current consumption decreases as the LO frequency is decreased, try decreasing the value of L4. After determining the optimum inductor value the current consumption should be minimized at the desired LO frequency.

2) Tune the LO port input network for optimum return loss.

Typically a bandpass network is used to pass the LO signal to the LOIN pin. It is desirable to block high frequency harmonics of the LO from the mixer core. LO harmonics will cause higher RF frequency images to be down converted to the desired IF frequency, and result in a degradation of sensitivity. If the intended LO source has poor harmonic distortion and spectral purity, it may be desirable to employ a higher order bandpass filter network. Figure 15 illustrates a simple L-C bandpass filter used to pass the fundamental frequency of the LO source. Capacitor C3 is a simple DC block, while the series-inductor, L3, along with the gate-to-source capacitance of the buffer amplifier form a low pass network. The native gate input of the LO buffer FET presents a rather high input impedance alone. The gate bias is generated internally using feedback which can result in a positive return loss at the intended LO frequency. It may be desirable to add shunt resistor to ground before the coupling capacitor C3 to present a lower loading impedance to the LO source if a better than -10dB return loss is desired.

3) Design the RF and IF filter networks.

Figure 15 depicts simple LC tank filter networks for the IF and RF port interfaces. The RF port LC network is designed to pass the RF input signal. The series LC tank has a resonant frequency at $1/(2\pi\sqrt{LC})$. At resonance the series reactances cancel, presenting a series short to the RF signal. A parallel LC tank is used on the IF port to reject the RF and LO signals. At resonance, the parallel LC tank presents an open circuit.

It is necessary to accommodate for the board parasitics and finite Q and self resonant frequencies of the LC components when designing the RF, IF and LO filter networks. Table 6 provides suggested values for initial prototyping.

Table 6. Suggested RF, IF and LO filter networks for low-side LO injection

RF Frequency	L1	C1	L2	C2	L3	C3
850MHz	6.8nH	4.7pF	4.7nH	5.6pF	8.2nH	100pF
1950MHz	1.7nH	1.5pF	1.7nH	1.2pF	3.5nH	100pF

EVALUATION BOARD

An evaluation board is available for the ADL5350. The evaluation board has two halves, a low-band designated as board A, and a high-band board designated as board B. The schematic for the evaluation board is presented in Figure 16.

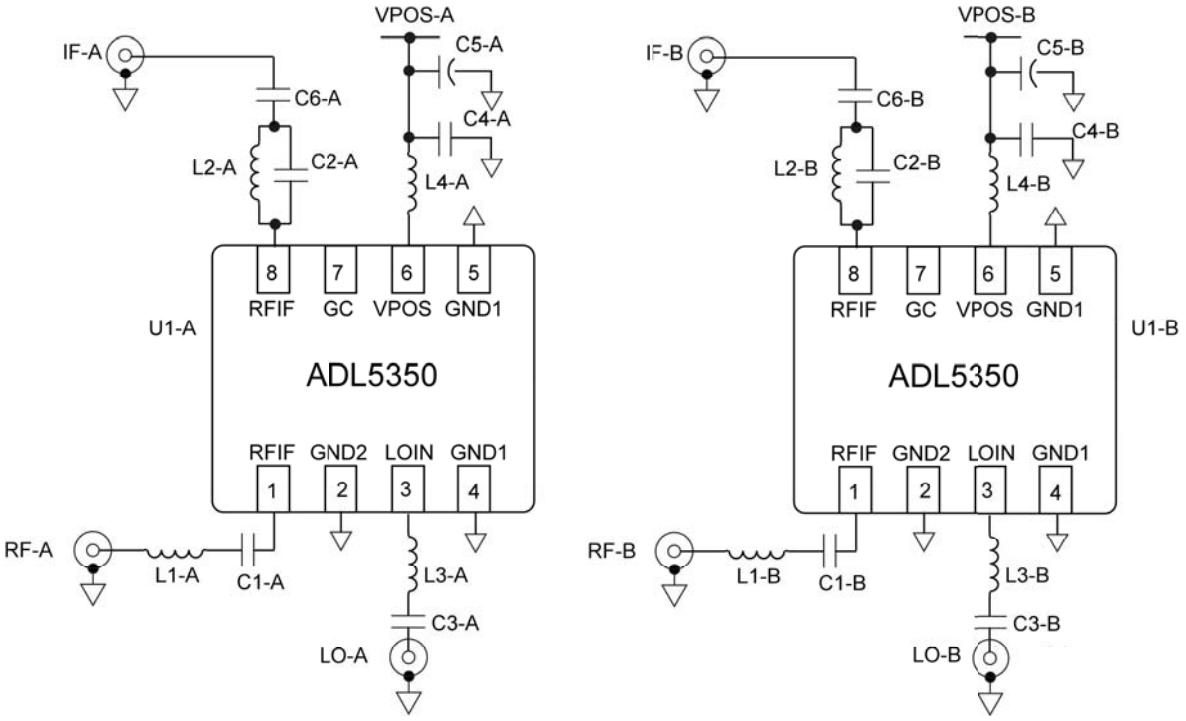

Figure16. Evaluation Board

Table 7. Evaluation Board Configuration Options

Component	Function	Default Conditions
C4-A, C4-B, C5-A, C5-B	Supply decoupling. C4-A and C4-B provide local bypassing of the supply. C5-A and C5-B are used to filter the ripple of a noisy supply line and are not always necessary.	C4-A = C4-B = 100pF C5-A = C5-B = 4.7µF
L1-A, L1-B, C1-A, C1-B	RF Input Network. Designed to provide series resonance at the intended RF frequency.	L1-A = 6.8nH (0603CS from Coilcraft) L1-B = 1.7nH (0302CS from Coilcraft) C1-A = 4.7pF C1-B = 1.5pF
L2-A, L2-B, C2-A, C2-B, C6-A, C6-B	IF Output Network. Designed to provide parrallel resonance at the geometric mean of the RF and LO frequencies.	L2-A = 4.7nH (0603CS from Coilcraft) L2-B = 1.7nH (0302CS from Coilcraft) C2-A = 5.6pF C2-B = 1.2pF C6-A = C6-B = 1nF
L3-A, L3-B, C3-A, C3-B	LO Input Netork. Designed to block DC and optimize LO voltage swing at LOIN.	L3-A = 8.2nH (0603CS from Coilcraft) L3-B = 3.5nH (0302CS from Coilcraft) C3-A = C3-B = 100pF
L4-A, L4-B,	LO Buffer Amp Choke. Provides bias and ac loading impedance to LO buffer amp.	L4-A = 24nH(0603CS from Coilcraft) L4-B = 3.8nH(0302CS from Coilcraft)

OUTLINE DIMENSIONS

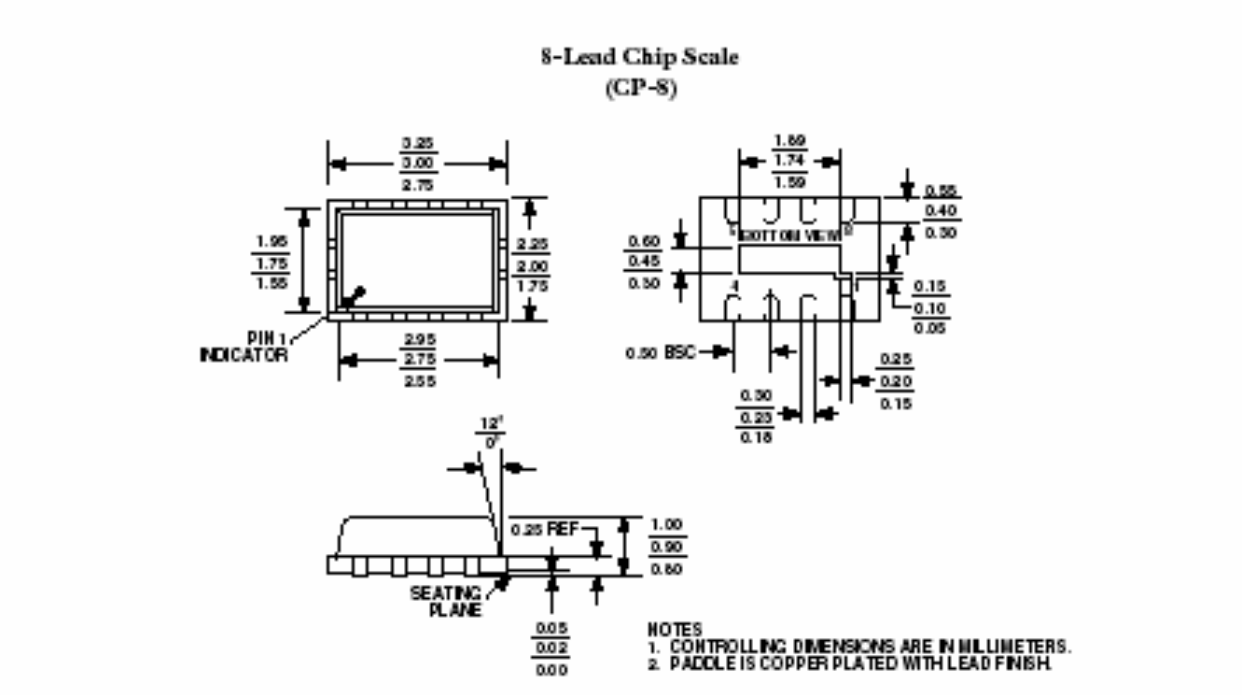

Figure 8. 8-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm × 2 mm Body (CP-8-3) Dimensions in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Outline	Branding
ADL5350ACPZ-REEL7[1]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package	CP-8-3	TBD
ADL5350ACPZ-WP[1,2]	−40°C to +85°C	8-Lead Lead Frame Chip Scale Package	CP-8-3	TBD
ADL5350-EVAL		Evaluation Board		

[1] Z = Pb-free part.
[2] WP = Waffle pack.

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